WHAT IS CLAIMED IS:

1. A fundamental cell, used as a basic unit in the layout of a semiconductor integrated circuit device, comprising:

no fixed wiring for commonly wiring between fundamental cells each other, and

connection terminals to be connected to upper wiring layers.

2. A fundamental cell according to claim 1, wherein:

wiring for wiring between the fundamental cells in the upper wiring layers.

3. A fundamental cell according to claim 1, further comprising:

more than two types of the connector terminals, wherein:

the wiring directions of wirings connected to the connector terminals and wired between the fundamental cells are in different wiring direction from each other including first and second directions perpendicular to each other.

4. A fundamental cell according to claim 1, wherein:

the connector terminals have the same wiring layers as the wirings to be wired between the fundamental cells.

5. A fundamental cell according to claim 1, wherein:

the connector terminals have stacked VIAs including the same wiring layers as the wiring to be wired between the fundamental cells.

6. A fundamental cell according to claim 1, wherein:

the wirings to be wired between the fundamental cells are wirings for interconnecting the fundamental cells, block cells having more than two of the fundamental cells to perform specific circuit operations, and macro cells having more than two of the block cells.

7. A fundamental cell according to claim 1, wherein:

the wirings to be wired between the fundamental cells includes

power source lines or ground potential lines,

the connector terminals include

power source terminals or ground potential terminals to the fundamental cell.

8. A semiconductor integrated circuit device, comprising:

a fundamental cell, used as a basic unit in a layout, having no fixed wiring to be commonly wired between the basic units, and having connector terminals to be connected to upper wiring layers; and

upper wirings in predetermined wiring directions and in predetermined wiring widths both appropriately selected, for connecting, in the upper wiring layers, the corresponding connector terminals of the fundamental cells.

9. A semiconductor integrated circuit device according to claim 8, wherein:

the upper wirings are made in a form of plane, in which the predetermined wiring widths exceed the fundamental cell.

10. A semiconductor integrated circuit device according to claim 8, wherein:

the upper wirings are formed by the wiring layers of other levels with respect to other lines or upper wirings over the other lines.

11. A semiconductor integrated circuit device according to claim 8, wherein:

the upper wirings form appropriately bypassing routes for bypassing around a wiring prohibited area present in a wiring path.

12. A wiring method, comprising the step of

wiring upper wirings at first by appropriately selecting the wiring directions and wiring widths of the upper wirings to be connected within upper wiring layers between the corresponding connecting

terminals of fundamental cells, for wiring a semiconductor integrated circuit device including more than two of the fundamental cells, which constitutes basic units in the layout design, having no fixed wiring to be placed in common between the basic units, and having connecting terminals to be connected to the upper wiring layers.

13. A wiring method according to claim 12, wherein:

the wiring widths of the upper wirings are defined in a form of a plane exceeding the fundamental cells.

14. A wiring method according to claim 12, wherein:

the upper wirings are defined in wiring layers of different levels with respect to other signal lines or upper wirings over the other lines.

15. A wiring method according to claim 12, wherein:

when there is present a wiring prohibited area on the wiring path of the upper wiring, the wiring prohibited area will be bypassed by routing appropriately the wiring path of the upper wiring.

16. A wiring method, comprising the step of:

wiring by performing an automatic wiring process of upper wirings together with other wirings, for wiring a semiconductor integrated circuit device including more than two of the fundamental cells, which constitutes basic units in the layout design, having no fixed wiring to be placed in common between the basic units, and having connecting terminals to be connected to the upper wiring layers.

17. A wiring apparatus for performing the wiring method according to claim 12, comprising:

a cell information storage unit for storing fundamental cell information including the positions of the connector terminals;

a wiring information configuration unit for configuring as

needed wiring information with respect to the wiring directions, wiring widths, wiring priority, wiring layers of the upper wirings to be connected with the corresponding connector terminals between the fundamental cells, as well as information with respect to wiring prohibited area in the wiring path;

a wiring information storage unit for storing wiring information configured by the wiring information configuration unit;

a controller unit for performing the wiring process in accordance with the information on the wiring directions, wiring widths, wiring priority, and wiring layers of the upper layer wirings stored in the wiring information storage unit and based on the position information of the connector terminals stored in the cell information storage unit for bypassing the wiring prohibited area in the wiring path;

a wiring monitoring unit for monitoring the progress of wiring process performed by the controller unit; and

a wiring data storage unit for storing the resulting wiring process performed by the controller unit.

18. A wiring apparatus for performing the wiring method according to claim 16, comprising:

a cell information storage unit for storing fundamental cell information including the positions of the connector terminals;

a wiring information configuration unit for configuring as needed wiring information with respect to the wiring directions, wiring widths, wiring priority, wiring layers of the upper wirings to be connected with the corresponding connector terminals between the fundamental cells, as well as information with respect to wiring prohibited area in the wiring path;

a wiring information storage unit for storing wiring information

configured by the wiring information configuration unit;

a controller unit for performing the wiring process in accordance with the information on the wiring directions, wiring widths, wiring priority, and wiring layers of the upper layer wirings stored in the wiring information storage unit and based on the position information of the connector terminals stored in the cell information storage unit for bypassing the wiring prohibited area in the wiring path;

a wiring monitoring unit for monitoring the progress of wiring process performed by the controller unit; and

a wiring data storage unit for storing the result of wiring process performed by the controller unit.